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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,484	10/17/2001	Edward G. Callway	00100.01.0069	6461

29153 7590 02/08/2007

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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/981,484	CALLWAY, EDWARD G.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,18-22 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,18,19,21,22 and 29-39* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1, 18, 19, 21, 22, and 29 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 3-4, filed August 7, 2006, with respect to the rejection(s) of claim(s) 1 and 18 under 35 U.S.C. 102(b) and claims 19, 21, 22, and 29 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Taylor (US006118461A) and Deering (US005963200A).

3. With regard to Claims 1 and 18, Applicant argues that the Normile (US005461679A) device teaches video compression and decompression modules, and does not teach graphics devices (page 2, paragraph 1).

In reply, the Examiner has made new grounds of rejection in view of Taylor, which more clearly teaches graphics devices. Taylor describes two display control units (103, Figure 1, Col. 4, lines 14-18), and each display control unit includes a display controller (104) and a frame buffer (105) (Col. 4, lines 19-21). A display controller is a VGA controller (Col. 4, line 49) and executes a limited number of graphics functions such as line draws, polygon fills, color space conversion, display data interpolation and zooming (Col. 4, lines 52-57).

Applicant argues that the office action alleges that the display 440 of Normile is a video output port. A display 440 is not a video output port since a display as known in the art is a display device (page 2, paragraph 2).

In reply, the Examiner disagrees. In Normile, since the first video component output 420 of the second graphics device 402 outputs video to display 440 (*information is placed onto bus 425 by modules 401-404, shared memory 405 is coupled to bus 425 and is further coupled to high speed "video" bus 420*, Col. 9, lines 20-24, 48-50; *frame buffer 430 may be directly coupled to the video bus 420, which frame buffer may then be coupled to a display such as 440*, Col. 10, lines 7-19), there must inherently be a video output port connected to display 440 in order to output the video to display 440.

4. With regard to Claim 19, Applicant argues that the connector of Jordan (US006028643A) is not an output node as claimed since the signals from the video monitor interface component 245 and 255 are not coupled to one another at a first output node and in fact the signals coming from the video monitor interface components 245 and 255 are routed in separate wires to two different monitors (page 3, paragraph 3).

In reply, the Examiner has made new grounds of rejection in view of Taylor, which more clearly teaches that the first signal and the second signal are provided to the same output node. Taylor describes a common port (109), operatively coupled to receive the first and second signals from either of the first (103a, Figure 1) and second (103b) graphics devices (*display driver 109 receives digital data from controller 104*, Col. 5, lines 1-3), as can be seen in Figure 1.

Applicant argues that the cited references also do not teach adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node (page 3, paragraph 4-page 4, paragraph 1).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Deering.

5. Applicant's arguments filed August 7, 2006, with respect to Claims 30-39 have been fully considered but they are not persuasive.

6. With regard to Claim 30, Applicant argues that Taylor teaches using different frame buffers and controllers to output sub-portions of a single screen. As such, entire frame display for each graphics device as claimed is not taught in the cited reference (page 2, paragraph 3-page 3, paragraph 1).

In reply, the Examiner disagrees. Since Taylor discloses each display controller renders video data for a frame buffer (Col. 5, line 65-Col. 6, line 1; Col. 6, lines 50-61; Col. 7, lines 11-30), and the well-known definition of a frame buffer is that a frame buffer stores video data for one frame, the display controllers each render respective frames of video. Claim 30 merely recites that each graphics device renders a frame, but does not specify that each frame is an entire display on a screen. Therefore, Taylor is considered to disclose the claim as it is written.

7. With regard to Claim 39, Applicant argues that Taylor does not describe adjacent frame control as required by the claim, but instead refers to outputting based on display control task partitioning, corresponding screen sub-portions (page 3, paragraph 2).

In reply, the Examiner disagrees. Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first and second rendered frames are adjacent frames of video. Since Claim 39 does not specify what the phrase "adjacent frames of video" means, the phrase "adjacent frames of video" is taken to mean that the second rendered frame is output immediately after the first rendered frame has been output, which is what Taylor teaches.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 30, 31, 38, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor (US006118461A).

10. With regard to Claim 30, Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). A frame buffer inherently stores an entire frame of information, and therefore each display control unit inherently generates entire frames of information. Therefore, Taylor describes an apparatus for providing video signals comprising a first graphics device operative to render a first frame of video and a second graphics device operative to render a second frame of video. Taylor describes a common port (109), operatively coupled to receive the first and second frames of rendered video from either of the first and second graphics devices (*display driver 109 receives digital data from controller 104*, Col. 5, lines 1-3), as can be seen in Figure 1. Since Taylor discloses each display controller renders video data for a frame buffer (Col. 5, line 65-Col. 6, line 1; Col. 6, lines 50-61; Col. 7, lines 11-30), and the well-known definition of a frame buffer is that a frame buffer stores video data for one frame, the display controllers each render respective frames of video. Claim 30 merely recites that each graphics device renders a frame, but does not specify that each frame is an entire display on a screen. Therefore, Taylor is considered to disclose the claim as it is written.

11. With regard to Claim 31, Taylor describes a first frame buffer operatively coupled to the first graphics device and a second frame buffer operatively coupled to the second graphics device (*two display control units 103, Col. 4, lines 14-18, each display control unit 103 includes a frame buffer 105*, Col. 4, lines 19-21).

12. With regard to Claim 38, Taylor describes that the first graphics device and second graphics devices (*two display control units 103*, Col. 4, lines 14-18) are video graphics adapters (*each display control unit 103 includes a display controller 104, Col. 4, lines 19-20, display controller 104 may be VGA controller*, Col. 4, line 49).

13. With regard to Claim 39, Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first and second rendered frames are adjacent frames of video. Since Claim 39 does not specify what the phrase "adjacent frames of video" means, the phrase "adjacent frames of video" is taken to mean that the second rendered frame is output immediately after the first rendered frame has been output, which is what Taylor teaches.

14. Thus, it reasonably appears that Taylor describes or discloses every element of Claims 30, 31, 38, and 39 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject

matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. Claims 1, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Normile (US005461679A).

18. With regard to Claim 1, Taylor discloses a video driver system comprising a first graphics device (103a, Figure 1; *two display control units 103, each display control unit 103 includes a display controller 104, each display controller 104 executes graphics functions such as line draws, polygon fills, color space conversion, display data interpolation and zooming, and video streaming,* Col. 4, lines 14-21, 52-57) having an input and a first video component output to provide a first video output component signal; a second graphics device (103b) having an input and a first video component output to provide a first video output component signal (*display controller 104 receives data, instructions and addresses across bus 102*, Col. 4, lines 50-52; *units 103 raster out data and refresh their corresponding screen regions*, Col. 5, line 65-Col. 6, line 1); a first video output port (109) coupled to the first video component output of the

first graphics device and the first video component output of the second graphics device (*display driver 109 receives digital data from controller 104*, Col. 5, lines 1-3), as can be seen in Figure 1.

However, Taylor does not teach a second video output port coupled to the first video component output of the second graphics device. However, Normile describes a video driver system comprising a first video device (401, Figure 4, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); a second video device (402, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (420) to provide a first video output component signal; a first video output port coupled to the first video component output of the first video device and the first video component output of the second video device (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426, shared memory 405 is coupled to bus 425 and is further coupled to high speed "video" bus 420*, Col. 9, lines 15-24, 48-50; *frame buffer 430 may be directly coupled to the video bus 420, which frame buffer may then be coupled to a display such as 440*, Col. 10, lines 7-19). Since the first video component output 420 of the second graphics device 402 outputs video to display 440

(Col. 9, lines 20-24, 48-50; Col. 10, lines 7-19), there must inherently be a video output port connected to display 440 in order to output the video to display 440. Therefore, there is a second video output port coupled to the first video component output of the second video device.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor to include a second video output port coupled to the first video component output of the second graphics device as suggested by Normile because Normile suggests the advantage of being able to output to two different displays at the same time (Col. 10, lines 7-19).

19. With regard to Claim 18, Taylor discloses a monitor (110, Figure 1) coupled to the first video output port (*DAC 109 receives digital data from controller 104 and outputs the analog data to drive display 110*, Col. 5, lines 1-3).

20. With regard to Claim 29, Taylor discloses a video driver system comprising a first graphics device (103a, Figure 1; Col. 4, lines 14-21, 52-57) having an input and a first video component output to provide a first video output component signal; a second graphics device (103b) having an input and a first video component output to provide a first video output component signal (Col. 4, lines 50-52; *units 103 raster out data and refresh their corresponding screen regions*, Col. 5, line 65-Col. 6, line 1); a first video output port (109) coupled to the first video component output of the first graphics device and to the first video component output of the second graphics device (*display driver 109 receives digital data from controller 104*, Col. 5, lines 1-3). Taylor describes that the frame from the frame buffer of display control unit 103a

(Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first graphics device renders a frame of video and provides the rendered frame to the first video output port, and that the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port. Since Taylor discloses each display controller renders video data for a frame buffer (Col. 5, line 65-Col. 6, line 1; Col. 6, lines 50-61; Col. 7, lines 11-30), and the well-known definition of a frame buffer is that a frame buffer stores video data for one frame, the display controllers each render respective frames of video. Claim 29 merely recites that each graphics device renders a frame, but does not specify that each frame is an entire display on a screen. Therefore, Taylor is considered to disclose the claim as it is written. Since Claim 29 does not specify what the phrase "adjacent frames of video" means, the phrase "adjacent frames of video" is taken to mean that the second rendered frame is output immediately after the first rendered frame has been output, which is what Taylor teaches.

However, Taylor does not teach a second video output port coupled to the first video component output of the second graphics device. However, Normile describes a video driver system comprising a first video device (401, Figure 4, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); a second video

device (402, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (420) to provide a first video output component signal; a first video output port (425) coupled to the first video component output of the first video device and the first video component output of the second video device (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24, 48-50; Col. 10, lines 7-19); and a second video output port (440) coupled to the first video component output of the second video device (Col. 10, lines 7-19). This would be obvious for the same reasons given in the rejection for Claim 1.

21. Claims 19, 21, 22, 32-34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Deering (US005963200A).

22. With regard to Claim 19, Taylor discloses a method of providing a video signal, the method comprising generating a first signal at a first device (103a, Figure 1; Col. 4, lines 14-21, 52-57), wherein the first signal is representative of a first video output component (Col. 5, line 65-Col. 6, line 1); providing the first signal to a first node (109); determining a value of the first signal at a first output node (*digital to analog converter pallete (display driver) 109 receives digital data from controller 104, and outputs analog data to drive display 110 in response*, Col. 5, lines 1-3); generating a second signal at a second device (103b), wherein the second signal is

representative of a first video output component (Col. 4, lines 52-57); providing the second signal of the second device to the first output node (Col. 5, lines 1-3).

However, Taylor does not teach adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node (*three systems, each of these systems includes a rendering controller 14,* Col. 3, lines 19-25; *system 1 is programmed to act as the master and system 2 is programmed to act as the slave, the master emits the FIELD signal and the slave systems receive it, system 1 becomes the source of the vertical interval timing reference, the slaves respond to the received FIELD signal by resetting the counters, the reset state is defined to be identical to the state which exists in the master RAMDAC at the time when it emits the transition in the FIELD signal,* Col. 5, lines 22-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor to include adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node as suggested by Deering because Deering suggests the advantage that the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate

from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

23. With regard to Claim 21, Taylor does not explicitly teach that the value of the first and second signals is a voltage value. However, Deering discloses that the value of the first and second signals is a voltage value (*RAMDAC 21 is coupled to the host bus through the rendering controller and translates data from the frame buffer to a signal which is converted by a DAC to analog signals representing voltage levels,* Col. 1, line 61-Col. 2, line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor so that the value of the first and second signals is a voltage value as suggested by Deering because Deering suggests that it is well-known in the art that the video output is controlled by voltage levels (Col. 1, line 61-Col. 2, line 2).

24. With regard to Claim 22, Taylor does not teach that the step of determining includes modifying and comparing the value of the first signal until the value of the first signal substantially matches a predetermined value. However, Deering discloses that the step of determining includes modifying and comparing the value of the first signal until the value of the first signal substantially matches a predetermined value (Col. 5, lines 22-45). This would be obvious for the same reasons given in the rejection for Claim 19.

25. With regard to Claim 32, Taylor describes at least one digital to analog converter (109, Figure 1) operatively coupled to output video (*digital to analog converter 109...outputs the analog data to drive display 110*, Col. 5, lines 1-3).

However, Taylor does not teach having voltage adjusted in order to correlate video out voltages being provided by at least one of the graphics devices. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node in order to correlate video out being provided by at least one of the graphics devices (Col. 3, lines 19-25; Col. 5, lines 22-45). Deering discloses that the value of the first and second signals is a voltage value (Col. 1, line 61-Col. 2, line 2). This would be obvious for the same reasons given in the rejection for Claims 19 and 21.

26. With regard to Claim 33, Taylor does not teach a circuitry operative to provide digital to analog conversion voltage equalization associated with the first and second graphics devices. However, Deering describes an apparatus for providing video signals comprising a first graphics device (14, Figure 2) operative to render a first frame of video and a second graphics device (14) operative to render a second frame of video. Deering describes a circuitry operative to provide digital to analog conversion frequency equalization (*synchronizes events produced in the video timing generator circuits of the three RAMDACs*, Col. 5, lines 12-16). The frequencies produced by the RAMDACs will vary within a range of values which depends on voltage (Col. 4, lines 57-63). Adjusting the frequency means adjusting the voltage. This is well-known in the art, and can

be found in many publications, such as Wunner (US005095280A) (*the VCO to adjust up or down to the new selected frequency*, Col. 8, lines 1-14). Therefore, Deering describes a circuitry operative to provide digital to analog conversion voltage equalization.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor to include a circuitry operative to provide digital to analog conversion voltage equalization associated with the first and second graphics devices as suggested by Deering because Deering suggests that a system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, it is advantageous to include a circuitry operative to provide digital to analog conversion frequency or voltage equalization because it avoids exhibiting aberrations in the viewed images.

27. With regard to Claim 34, Taylor describes selecting video from the second graphics device (103b, Figure 1) to be output to the common port (*display driver 109 receives digital data from controller 104, Col. 5, lines 1-3, MAP OUT port of display unit 103b is then set active*, Col. 7, lines 25-30).

However, Taylor does not teach that the first graphics device includes a controller operative to select video from the second graphics device to be output. However, Deering describes a master graphics device and a slave graphics device (Col. 5, lines 22-25). The master graphics device emits the FIELD signal and the slave graphics device receives it (Col. 5, lines 25-27). The slave graphics device responds to the received FIELD signal by resetting the

counters which produce the video timing signals (Col. 5, lines 30-33). Therefore, Deering describes that the first graphics device includes a controller operative to select video from the second graphics device to be output.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor so that as suggested by Deering because Deering suggests that this is how a master-slave system works (Col. 5, lines 22-33). Deering suggests that a master-slave system is advantageous because the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

28. With regard to Claim 36, Taylor does not teach that the first graphics devices acts as a master to the second graphics device and provides synchronization control for the second graphics device. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and provides synchronization control for the second graphics device (Col. 3, lines 19-25; *the slaves respond to the received FIELD signal by resetting the counters which produces the video timing synch signals, the reset state is defined to be identical to the state which exists in the master RAMDAC at the time when it emits the transition in the FIELD signal, thus achieving the required synchronization*, Col. 5, lines 22-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor so that the first graphics devices acts as a master to the second graphics device and provides synchronization control for the second graphics device as suggested by Deering because Deering suggests the advantage that the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

29. With regard to Claim 37, Taylor does not teach that the first graphics device includes a reference signal generator for the second graphics controller. However, Deering describes that the first graphics devices includes a reference signal generator for the second graphics controller (*system 1 becomes the source of the vertical interval timing reference*, Col. 5, lines 22-45), as discussed in the rejection for Claim 36.

30. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Eichenberger (see Prior Art of Record below).

Taylor is relied upon for the teachings as discussed above relative to Claim 30.

However, Taylor does not teach a load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving the common port. However, Eichenberger describes the use of a dummy switch with a load

coupled to it for charge cancellation of the active switch (pp. 257, 260). In other words, the switch that is not active or is not driving the common port acts as the dummy switch and has a load coupled to it.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor to include a load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving the common port as suggested by Eichenberger because Eichenberger suggests the advantage of reducing charge injection by charge cancellation (page 257). The advantages of using dummy switches is well-known in the art and can be found in many publications.

Allowable Subject Matter

29. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

30. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a method comprising the step of removing the first signal from the first node prior to the step or providing the second signal as recited in Claim 20. This claim is similar to Claim 19 of U.S. patent 6,424,320, to which this application is a continuation of.

Prior Art of Record

C. Eichenberger, W. Guggenbuhl, "On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 256-264, 1990.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kehlet (US005956046A) describes a video system comprising a first frame buffer (202A, Figure 3) having an input (Col. 5, lines 49-51) and a first video component output (222A) to provide a first video output component signal (Col. 5, lines 51-53); a second frame buffer (202B) having an input (Col. 5, lines 49-51) and a first video component output (222B) to provide a first video output component signal (Col. 5, lines 51-53); a first video output port (220) coupled to the first video component output of the first frame buffer and to the first video component output of the second frame buffer (Col. 5, lines 51-53); wherein the first frame buffer has a rendered frame of video and provides the rendered frame to the first video output port, and wherein the second frame buffer has a rendered adjacent frame of video and provides the adjacent frame to the first video output port (Col. 6, lines 13-22).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER